SUBJECT : Digital Electronics and Microprocessor (Theory)

Semester From Date:**01.07.2026** To Date: **05.11.2026**

LESSON PLAN

Prepared by: Udaya Meher, Lecturer Stage-I, ETC

COURSE OUTCOMES (COs):

- CO1: Apply digital fundamentals, Boolean algebra and its applications in simple digital systems.
- CO2: Comprehend combinational logic circuits.
- CO3: Illustrate analysis and design procedures for synchronous and asynchronous sequential circuits.
- CO4: Explain the various semiconductor memories and related technology.
- CO5: Explain the architecture of microprocessor 8085.

CO-PO MAPPING:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO1	3	3	2	1	1		
CO2	3	3	3	2	1		
CO3	3	3	3	3	2		
CO4	3	2	2	2	2		
CO5	3	2	2	2	3		

WEEKLY LESSON PLAN:

Discipline	Electrical Engg.	Semester	5th
Subject	Digital Electronics and Microprocessor	Course Code	EEPC301
Theory/No of days/week	3	No of weeks	17
Total Contact Hours	45 Hrs	Credit	3

Week	Class day	Theory topic	CO
1	1st	Digital Fundamentals: Number Systems - Decimal, Binary, Octal, Hexadecimal	CO1
1	2nd	1s and 2s complements, Codes - Binary, BCD, Excess 3, Gray	CO1
1	3rd	Alphanumeric codes, Boolean theorems	CO1
2	1st	Logic gates and truth tables, Universal gates	CO1
2	2nd	Sum of products and product of sums, Minterms and Maxterms	CO1
2	3rd	Karnaugh map Minimization	CO1
3	1st	QuineMcCluskey method of minimization	CO1
3	2nd	Revision and Unit Test	CO1
3	3rd	Combinational & Synchronous Sequential Circuits: Half and Full Adders	CO2
4	1st	Half and Full Subtractors, Binary Parallel Adder	CO2
4	2nd	Multiplexer, Demultiplexers, Decoders	CO2
4	3rd	Priority Encoder	CO2

5	1st	Flip flops - SR, JK, T, D	CO2
5	2nd	Design of clocked sequential circuits	CO2
5	3rd	Design of Counters	CO2
6	1st	Shift registers, Universal Shift Register	CO2
6	2nd	Revision and Unit Test	CO2
6	3rd	Asynchronous Sequential Circuits: Stable and Unstable states, output specifications	CO3
7	1st	Cycles and races, state reduction	CO3
7	2nd	Race free assignments, Hazards, Essential Hazards	CO3
7	3rd	Pulse mode sequential circuits, Design of Hazard free circuits	CO3
8	1st	Memory Devices: Basic memory structure - ROM, PROM, EPROM, EEPROM	CO4
8	2nd	RAM - Static and dynamic RAM	CO4
8	3rd	Programmable Logic Devices - PLA, PAL, FPGA	CO4
9	1st	Revision and Unit Test	CO3, CO4
9	2nd	8085 Processor: Hardware Architecture, pin diagram	CO5
9	3rd	Functional Building Blocks of Processor	CO5
10	1st	Memory organization	CO5
10	2nd	I/O ports and data transfer concepts	CO5
10	3rd	Timing Diagram	CO5
11	1st	Interrupts	CO5
11	2nd	Revision and Unit Test	CO5
11	3rd	Programming Processor: Instruction format and addressing modes	CO5
12	1st	Assembly language format	CO5
12	2nd	Data transfer, data manipulation & control instructions	CO5
12	3rd	Programming: Loop structure with counting & Indexing	CO5
13	1st	Look up table	CO5
13	2nd	Subroutine instructions, stack	CO5
13	3rd	8255 architecture and operating modes	CO5
14	1st	8255 operating modes and applications	CO5
14	2nd	Problem solving and numericals	CO5
14	3rd	Problem solving and numericals	CO5
15	1st	Revision - Unit I & II	CO1, CO2
15	2nd	Revision - Unit III & IV	CO3, CO4, CO5
15	3rd	Revision - Unit V	CO5
16	1st	REVISION	All COs
16	2nd	REVISION	All COs
16	3rd	REVISION	All COs
17	1st	REVISION	All COs
17	2nd	REVISION	All COs
17	3rd	REVISION	All COs

Teacher Sign 29/6/26

HoD, Electrical Engg. 29-06-26