LESSON PLAN

Department: CSE		Semester: 3rd , Name of Faculty : MANAS RANJAN PATTI
Subject: Digital Electronics (DE)	No. of days/ week Class allotted: 4	Effective From Date: 01.07.2024
		No. of Week- 15
		Topic to be Covered:
Week	**Class Day**	**Theory**
1st	1st	**UNIT 1: BASICS OF DIGITAL ELECTRONICS**
	2nd	**1.1.** Number System-Binary, Octal, Decimal,
	3rd	Hexadecimal - Conversion from one system to another number system.
	4th	**1.2** Arithmetic Operation-Addition, Subtraction, Multiplication, Division,
2nd	1st	1‟s & 2‟s complement of Binary numbers& Subtraction using complements method.
	2nd	**1.3** Digital Code & its application & distinguish between weighted & non-weight Code,
	3rd	Binary codes, excess-3 and Gray codes.
	4th	**1.4** Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR—Symbol,
3rd	1st	Function, expression, truth table & timing diagram
	2nd	**1.5** Universal Gates& its Realization
	3rd	**1.6** Boolean algebra, Boolean expressions, Demorgan‟s Theorems.
	4th	**1.7** Represent Logic Expression: SOP & POS forms
4th	1st	**1.8** Karnaugh map (3 & 4 Variables)&Minimization of logical expressions, don‟t care conditions
	2nd	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
	3rd	**UNIT-2: COMBINATIONAL LOGIC CIRCUITS**
	4th	**2.1** Half adder, Full adder,
5th	1st	Half Subtractor, Full Subtractor,
	2nd	Serial and Parallel Binary 4 bit adder.
	3rd	**2.2** Multiplexer (4:1),
	4th	De- multiplexer (1:4), Decoder, Encoder,
6th	1st	Digital comparator (3 Bit)
	2nd	**2.3** Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above).
	3rd	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
	4th	**UNIT-3: SEQUENTIAL LOGIC CIRCUITS**
7th	1st	**3.1** Principle of flip-flops operation, its Types,
	2nd	**3.2** SR Flip Flop using NAND,NOR Latch (un clocked)
	3rd	**3.3** C l o c k e d SR,D,JK,T,JK Master Slave flip-flops-Symbol,
	4th	logic Circuit, truth table and applications

8th	**1st**	**3.4** Concept of Racing and how it can be avoided.
	2nd	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
	3rd	**UNIT-4: REGISTERS, MEMORIES & PLD**
	4th	**4.1** Shift Registers-Serial in Serial -out, Serial- in Parallel-out,
9th	**1st**	Parallel in serial out and Parallel in parallel out
	2nd	**4.2** Universal shift registers-Applications.
	3rd	**4.3** Types of Counter & applications
	4th	**4.4** Binary counter, Asynchronous ripple counter (UP & DOWN),
10th	**1st**	Decade counter. Synchronous counter, Ring Counter.
	2nd	**4.5** Concept of memories-RAM, ROM,
	3rd	static RAM, dynamic RAM,PS RAM
	4th	**4.6** Basic concept of PLD & applications
11th	**1st**	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
	2nd	**UNIT-5: A/D AND D/A CONVERTERS**
	3rd	5.1 Necessity of A/D and D/A converters.
	4th	**5.2** D/A conversion using weighted resistors methods.
12th	**1st**	**5.3** D/A conversion using R-2R ladder (Weighted resistors) network.
	2nd	**5.4** A/D conversion using counter method.
	3rd	**5.5** A/D conversion using Successive approximate method
	4th	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
13th	**1st**	**Unit-6: LOGIC FAMILIES**
	2nd	**6.1** Various logic families &categories according to the IC fabrication process
	3rd	**6.2** Characteristics of Digital ICs- Propagation Delay,
	4th	fan-out, fan-in, Power Dissipation,
14th	**1st**	Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
	2nd	**6.3** Features, circuit operation &various applications of TTL(NAND),
	3rd	CMOS (NAND & NOR)
	4th	**1. Doubt Clearing class** **2. Quiz test** **3. Assignment**
15th	**1st**	**Revision**
	2nd	**Revision**
	3rd	**Previous Year Question Discussions**
	4th	**Previous Year Question Discussions**

Signature of Faculty

HOD
Senior Lecture, CSE
Govt. Polytechnic,
Kandhamal